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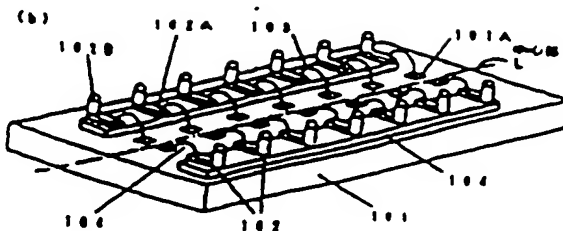
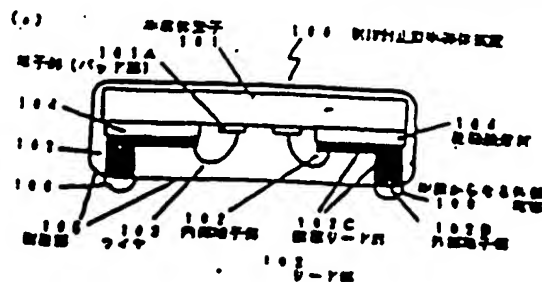
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(51) (発明の名称) 積層型半導体装置とそれを用いられるリードフレーム、及び積層型半導体装置の製造方法

(52) (要約)

【目的】 更なる積層型半導体装置の高集積化、高信頼化が求められている中、半導体装置パッケージサイズにおけるチップの占有率を上げ、半導体装置の小型化に対応させ、同時に従来の T S O P 等の小型パッケージに類似であった更なる多ピン化を実現した積層型半導体装置を提供する。

【構成】 半導体装置の電子側の面に、半導体装置の電子と電気的に接続するための内部端子部と、半導体装置の電子側の面へ固定して外部へと向く外部端子部への接続のための外部端子部と、前記内部端子部と外部端子部とを接続する接続リード部とを一体とした装置のリード部とを、絶縁性材料層を介して、固定して設けてあり、且つ、前記基板等への実装のための半田からなる外部電極を前記装置の各リードの外周端子部に接続させ、少なくとも前記半田からなる外部電極の一部は装置部より外部に突出させて設けている。



(U F H J C K E)

(拾遺項1) 本式は親子の親子間の正に 二通は親子の親子と親子間には納するたの外面親子間と、本通は親子の親子間の正へ通交して外親へと向く外親回帰への修成のための外面親子間と、内記内親親子間と外親親子間とを連結するは親リード部とを一体としたリード部を構成部、他は修成費用を介して、並列してはいており、且つ、回帰部等への実交のための本田からなる外親回帰部と内記修成部をリードの外親親子間に連結させ、少なくとも内記本田からなる外親回帰部の一部に修成部より外親に並列させて設けていることを以てする取捨停止部を構成部とす。

(註本厚2) 註本厚1において、半導体素子の結子は半導体素子の結子面の一対の辺の結子中心距離上にあって配置されており、リード線は結子の結子を挟むように対向し結子一対の辺に接し付けられていることを特徴とする出願防止型半導体装置。

(建設項 3) 本磁気素子の磁子と電気的に接続するための内部磁子部と、外部回路と接続するための外装磁子部と、前述内部磁子部と外装磁子部とを連結する接続リード部とを一体とし、以外装磁子部を、接続リード部を介して、リードフレーム面から固定する一方、面に出させ、対向し先端部同士で連結部を介して接続する一方、内部磁子部を接続付けており、且つ、各外装磁子部の先端部、接続リード部と連結し、一体として全体を露出する外装部を設けていることを特徴とするリードフレ-

(図2項4) 半導体素子の端子側の面に、半導体素子の電極と電気的に接続するための内部端子部と、半導体素子の端子側の面へ重交して外部へと向く外部配線への接続のための外部端子部と、前記内部端子部と外部端子部とを接続する積成リード部とを一体とした積成のリード部とを、絶縁層形成層を介して、露出させて設けてお、且つ、配線基板等への実装のための半田からなる外電極を前記積成の各リードの外周端子部に接続させ、なくとも前記半田からなる外周電極の一部は露出部より外部に露出させて設けている積成防止型半導体装置の他方法であつて、少なくとも、(A)エッチング加工で、半導体素子の電極と電気的に接続するための内部端子部と、外部配線と接続するための外部端子部と、両者部端子部と外部端子部とを接続する積成リード部とを一体とし、該外部端子部を、積成リード部を介して、リードフレーム面から重交する一方所部に露出させ、外周配線露出と導通部を介して接続する一方の外電極とを露出設けており、且つ、各外部端子部の外側で、リード部と接続し、一体として全体を露出する方向に設けているリードフレームを作製する工程、(B)リードフレームの外周端子部側でない面(裏面)に材料を設け、打ち抜き金型により、外周する内周端子部を接続する導通部と該導通部に対応する位置に設

けられた鉄板を閉じ、リッドフレームのにもり
かれた部分が生じるとは必然にこうにして、
たけを介して、リッドフレーム全体を正確に
固定する工程。(C)リッドフレームの内部
の部分を閉じ、金具による取付け工程。

(見解の異なる点)

(0001)

(産業上の利用方針) 本発明は、半導体素子を含む素子部を封止型の半導体パッケージ(プラスチックパッケージ)に封止し、特に、高湿度区画に用いられ、かつ、多ピン化に対応できる半導体装置とその封止方法に関する。

(0 0 0 2)

10 【従来の技術】近年、半導体装置は、高集積化、小型化、高速度化の進歩と電子機器の高性能化と高度集積化の傾向（時代）から、LSIのASICに代替されるように、ますます高集積化、高速度化になってきている。これに伴い、リードフレームを用いた封止型の半導体装置ブラケットパッケージにおいても、その集積のトレンドが、SOJ (Small Outline)-Lead Package や QFP (Quad Flat Package) のような高集積型のパッケージを経て、TSOP (Thin Small Outline Package) の集積による薄型化を主軸としたパッケージの小型化へ、さらにはパッケージ内部の3次元化によるチップ収容効率向上を目的としたLOC (Lead On Chip) の集積へと進展して来た。しかし、密封型半導体装置パッケージには、高集積化、高速度化とともに、更に一層の多ピン化、薄型化、小型化が求められており、上記従来のパッケージにおいてもチップ表面部分のリードの引き出しがあるため、パッケージの小型化に障壁が見えて来た。また、TSOP等の小型パッケージにおいては、リードの引き出し、ピンピッチから多ピン化に対しても障壁が見えて来た。

(0 0 0 2)

「説明が解決しようとする課題」上記のように、更なる
用器防止型半導体装置の高集積化、高信頼化が求めら
れており、新設計防止型半導体装置パッケージの一角の多ピン
化、用器化、小型化が求められている。本説明は、こ
のような状況のもと、半導体装置パッケージサイズにお
けるチップの占有率を上げ、半導体装置の小型化に対応
させ、回路基板への実装密度を低減できる、即ち、回路
基板への実装密度を向上させることができる用器防止型
半導体装置を提供しようとするものである。また、既述

に従来の T S O P 系の小型パッケージに搭載であった更なる多ピン化を要求しようとするものである。

(0 0 0 4)

(用途を解放するための手段) 本発明の断端防止型半導体装置は、半導体素子の端子側の面に、半導体素子の端子と電気的に接続するための内部端子部と、半導体素子の端子側の面へ突出して外部へと向く外部端子部への接続のための外部端子部と、前記内部端子部と外部端子部とを連結する接続リード部とを一体とした複数のリード部とを、絶縁基板層を介して、露出して設けており、且つ、絶縁基板層への突出のための半田からなる外部電極を前記複数の各リードの外部端子部に接続させ、少なくとも前記半田からなる外部電極の一部は断端より外部に突出させて設けていることを特徴とするものである。尚、上記において、内部端子部と外部端子部とを一体とした複数のリード部の配列を半導体素子の端子側面に二次元的に配列し、外部電極部を半田ボールにて形成することにより B C A (B a l l G r i d A r r a y) タイプの断端防止型半導体装置とすることとする。

(0 0 0 5) そして、上記において、半導体素子の端子は半導体素子の端子側の面の一列の辺の中心位置上にそって配置されており、リード部は複数の端子を挟むように対向し前記一列の辺に沿って設けられていることを特徴とするものである。また、本発明のリードフレームは、断端防止型半導体装置用のリードフレームであって、半導体素子の端子と電気的に接続するための内部端子部と、外部端子部とを連結するための外部端子部と、前記内部端子部と外部端子部とを連結する接続リード部とを一体とし、該外部端子部を、接続リード部を介して、リードフレーム面から突出する一方の側に突出させ、対向し先端部同士で接続部を介して接続する一方の内部端子部を接続設けており、且つ、各外部端子部の外側で、接続リード部と連絡し、一体として全体を保持する外側部を設けていることを特徴とするものである。尚、上記リードフレームにおいて、内部端子部と外部端子部とをそれぞれを連結する接続リード部とを一体とした複数の接続リードフレーム面に二次元的に配列するとして形成することにより B C A (B a l l G r i d A r r a y) タイプの断端防止型半導体装置用のリードフレームとすることとする。

(0 0 0 6) 本発明の断端防止型半導体装置の製造方法は、半導体素子の端子側の面に、半導体素子の端子と電気的に接続するための内部端子部と、半導体素子の端子側の面へ突出して外部へと向く外部端子部への接続のための外部端子部と、前記内部端子部と外部端子部とを連結する接続リード部とを一体とした複数のリード部とを、絶縁基板層を介して、露出して設けており、且つ、絶縁基板層への突出のための半田からなる外部電極を前記複数の各リードの外部端子部に接続させる工程と、

前記半田からなる外部電極の一部は断端より外部に突出させて設ける工程とを有する工程を有する製造方法であって、少なくとも、(A) エッチング加工にて、半導体素子の端子と電気的に接続するための内部端子部と、外部端子部とを連結するための外部端子部と、前記内部端子部と外部端子部とを連結する接続リード部とを一体とし、該外部端子部を、接続リード部を介して、リードフレーム面から突出する一方の側に突出させ、対向し先端部同士で接続部を介して接続する一方の内部端子部を接続設けており、且つ、各外部端子部の外側で、接続リード部と連絡し、一体として全体を保持する外側部を設けているリードフレームを形成する工程、(B) 前記リードフレームの外部端子部側でない面(裏面)に絶縁層を設け、前記絶縁層により、対向する内部端子部同士を接続する接続部と外部端子部とに接続する位置に設けられた絶縁層を開口させ、リードフレームの開口部が形成された部分が半導体素子の端子部にくるようにして、前記半導体素子を介して、リードフレーム全体を半導体素子へ搭載する工程、(C) リードフレームの外側部を含む不要の部分を開口部を金型により切断する工程、(D) 半導体素子の端子部と、切断されて、半導体素子へ搭載された内部端子部の先端部とをワイヤボンディングした後に、断端により外部端子部側のみを外部に突出させて全体を封止する工程、(E) 前記外部部に突出した外部端子部面に半田からなる外部電極を形成する工程、とを含むことを特徴とするものである。

(0 0 0 7)

(作用) 本発明の断端防止型半導体装置は、上記のような構成にすることにより、半導体装置パッケージサイズにおけるチップの占率を上げ、半導体装置の小型化に対応できるものとしている。即ち、半導体装置の内部端子部への突出電極を形成し、絶縁基板への突出電極の向上を可能としている。詳しくは、内部端子部、外部端子部とを一体とした複数のリード部を半導体素子部に絶縁層から開口させて露出し、前記外部端子部に半田からなる外部電極部を接続させていることより、装置の小型化を達成している。そして、上記半田からなる外部電極部を、半導体素子面に絶縁層を二次元的に配列することにより、半導体装置の多ピン化を可能としている。半田からなる外部電極部を半田ボールとし、二次元的には外部電極部を配列した場合には B C A タイプとなり、半導体装置の多ピン化にも対応できる。また、上記において、半導体素子の端子が半導体素子の端子側の面の一列の辺の中心位置上にそって配置され、リード部は複数の端子を挟むように対向し前記一列の辺に沿って設けられており、簡単な構造とし、製造性に優れた構造としている。本発明のリードフレームは、上記のような構成にすることにより、上記断端防止型半導体装置の製造を可能とするものであるが、通常のリードフレームと同様のエッチ

の平直部を図2に示すリードフレームを作製した(図3(c))。図2(b)のは、図2(a)～a2における平直部である。これは、レジストを剥離した後、洗浄処理を施した後、所定の箇所(内部端子部分を含む領域)のみに金メッキ処理を行った。(図3(e))。尚、上記リードフレームの製造工程においては、図2(b)に示すように、外部部と内部部を形成するための、外部部形成面からのエッチング(露出)を多く行い、反対面側からは少なめにエッチング(露出)を行った。また、金メッキに代り、銀メッキやパラジウムメッキでも良い。上記のリードフレームの製造方法は、1ヶの半導体装置を作製するために必要なリードフレーム1ヶの製造方法であるが、通常は半導体装置の面から、リードフレーム部材をエッチング加工する時、図2に示すリードフレームを複数個面付けした状態で作製し、上記の工程を行う。この場合は、図2に示す外部部205の一部に露出する導線(図示していない)をリードフレームの外側に露出させて露出状態とする。

(0011)次に、上記のようにして作製されたリードフレームを用いた、本発明の露出型半導体装置の製造方法の実施例を図に示して説明する。図4は、本発明の露出型半導体装置の製造工程を示すものである。図3に示すようにして作製されたリードフレーム400の外部端子部402形成面(下面)と対向する面に、ポリイミド系熱硬化型の絶縁性材料(テープ)401(日立化成株式会社製、HM122C)を、400°C、6Kg/cm²で1.0秒間圧着して貼りつけた(図4(a))。この状態の平面図を図5に示す。この状態では、図4(a)の平面図を以て図4(b)とし、対向する内部端子部の先端部を露出する導線部403と、その部分の絶縁性材料(テープ)401とを切り取った。(図4(c))

次いで、外周部404および圧着部406A、406Bを用い、外周部404を含む不要の部分を切り離す(図4(d))と同時に、絶縁性材料404を介して半導体素子407上にリード部408の圧着を行った。(図4(e))

尚、この図4(d)に示す、作製リードと露出してリードフレーム全体を支えている外部部204を含む不要の部分を切り離しは、露出型半導体装置に付しても良い。この場合には、通常の露出型半導体装置を用いたQFPパッケージ等のようにダムバー(図示していない)を設けると良い。リード部410を半導体素子411へ露出した後、ワイヤ414により、半導体素子の端子(パッド)411Aとリード部410の内部端子410Aとを電気的に接続した。(図4(f))

その後、所定の金型を用い、エポキシ系の樹脂415でリード部410の外部端子部410Bのみを固定させ、全体を封止した。(図4(g))

ここでは、導線の金型(図示していない)を用いたが、

所定の面(外部端子部)を露出し露出型半導体装置としし金型に必要としない。次いで、露出型半導体装置は素子部410B上に半導体素子をスクリーン印刷により露出し、半導体素子(ペースト)からなる外部端子部416を作製し、本発明の露出型半導体装置を作製した。(図4(h))

尚、半導体素子部416の作製は、スクリーン印刷に限定されるものではなく、リフローまたはポッティング等でも、図4(h)と半導体素子の作製に必要となる半導体素子が得られれば良い。

(0012)

【発明の効果】本発明は、上記のように、更なる露出型半導体装置の小型化、高信頼化が求められる状況のもと、半導体装置パッケージサイズにおけるチップの占有部を上げ、半導体装置の小型化に対応させ、図4(h)への露出部を露出させる、即ち、図4(h)への露出部を向上させることが出来る半導体装置の提供を可能としたものであり、同時に従来のT SOP等の小型パッケージに適用であった更なる多ピン化を実現した露出型半導体装置の提供を可能としたものである。

【図面の簡単な説明】

【図1】本発明の露出型半導体装置の概略図

【図2】本発明のリードフレームの平面図

【図3】本発明のリードフレームの製造工程図

【図4】本発明の露出型半導体装置の製造工程図

【図5】本発明のリードフレームに絶縁性材料を貼り付けた状態の平面図

【符号の説明】

100	露出型半導体装置
101	半導体素子
101A	端子部(パッド部)
102	リード部
102A	内部端子部
102B	外部端子部
102C	作製リード部
103	ワイヤ
104	絶縁性材料
105	樹脂部
106	半導体素子(ペースト)からなる外部

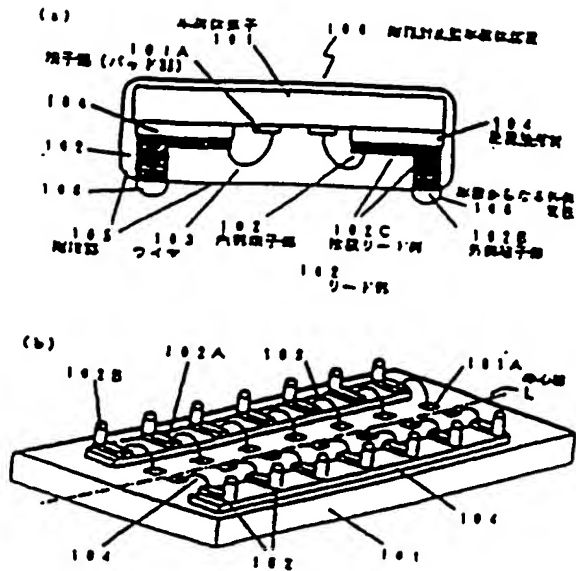
200	リードフレーム
201	内部端子部
202	外部端子部
203	作製リード部
204	導線部
205	外部部
300	リードフレーム部材
301	レジスト

74-100-10000

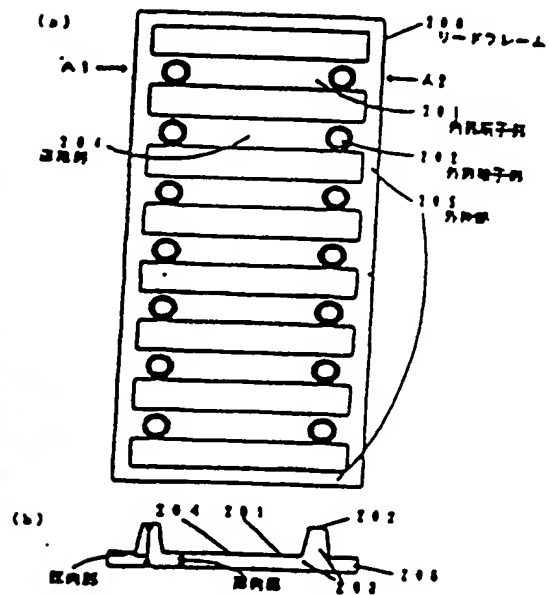
303A	内訳明子郎
303B	外訳明子郎
304	正位郎
305	金メッキ郎
306	外訳郎
400	リードフレーム
401	外訳明子郎 (テープ)
402	外訳明子郎
403	正位郎

405A. 405E	17ちびとせ
406A. 406B	たの17ちびとせよじに本用せ
410	リード紙
410A	内紙用子紙
410B	外紙用子紙
410C	増紙リード紙
411	半通作子
411A	ワイヤー
415	紙用

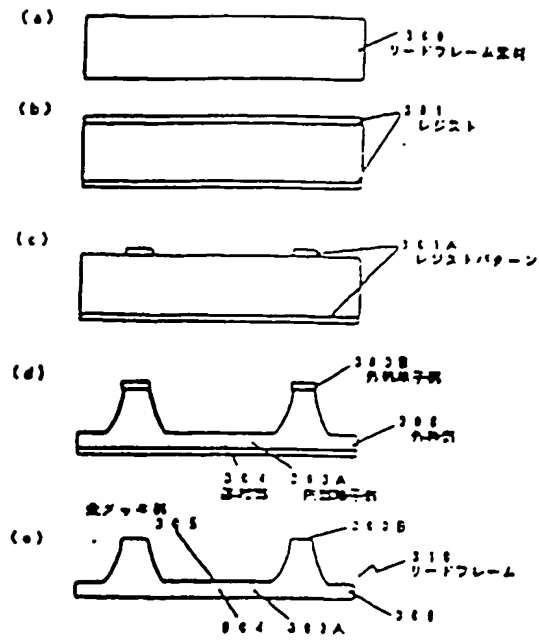
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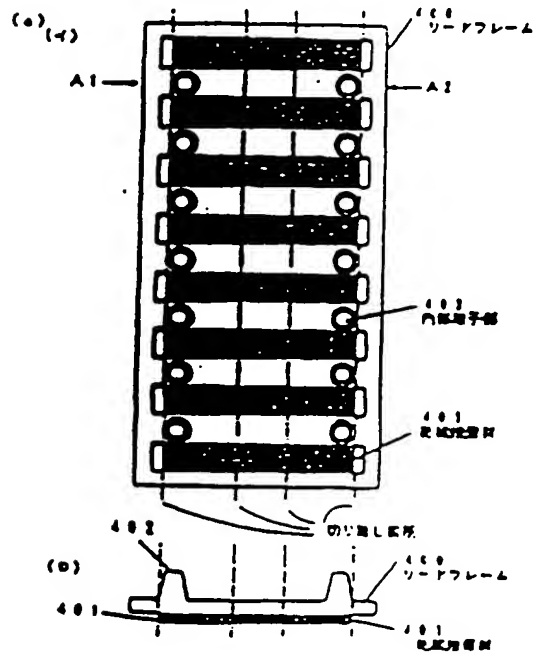
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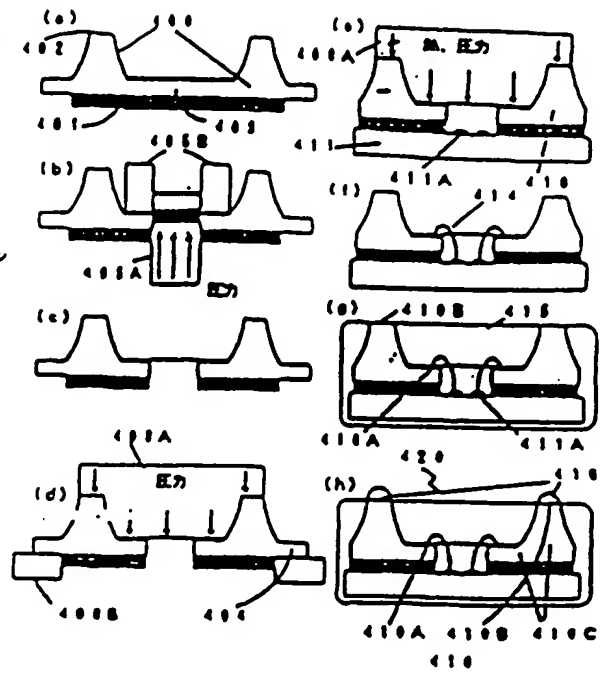
(図 3)



(図 5)



(図 4)



Japanese Patent Laid-Open Publication No. Heisei 8-125066

[TITLE OF THE INVENTION]

Resin Encapsulated Semiconductor Device, Lead Frame
5 Used Therein, and Fabrication Method for the Resin
Encapsulated Semiconductor Device

[CLAIMS]

1. A resin encapsulated semiconductor device
10 comprising:
a semiconductor chip;
a plurality of leads fixedly attached to a terminal-
end surface of the semiconductor chip by an insulating
adhesive interposed between the semiconductor chip and the
15 leads, each of the leads including integral portions, that
is, an inner terminal portion adapted to be electrically
connected to an associated one of terminals of the
semiconductor chip, an outer terminal portion extending
outwardly in a direction orthogonal to the terminal-end
20 surface of the semiconductor chip and adapted to be
connected to an external circuit, and a connecting lead
portion adapted to connect the inner and outer terminal
portions to each other; and
outer electrodes each connected to the outer terminal
25 portion of an associated one of the leads and made of

solder to allow the semiconductor device to be mounted on a circuit board, at least a part of the outer leads being externally exposed from a resin encapsulate.

5 2. The resin encapsulated semiconductor device according to claim 1, wherein the terminals of the semiconductor chip are arranged along a substantially center line between a pair of sides of the semiconductor chip on the terminal-end surface of the semiconductor chip,
10 and the leads are arranged in two facing sets along the sides of the semiconductor chip, respectively, in such a fashion that the terminals of the semiconductor chip are interposed between the two facing lead sets.

15 3. A lead frame comprising:

 a plurality of leads each including integral portions, that is, an inner terminal portion adapted to be electrically connected to an associated one of terminals of a semiconductor chip, an outer terminal portion adapted to
20 be connected to an associated one of terminals of an external circuit, and a connecting lead portion adapted to connect the inner and outer terminal portions to each other;

 each of the outer terminal portions of the leads
25 being protruded in a direction orthogonal to a lead frame

surface via an associated one of the connecting lead portions;

the inner lead portions of the leads being arranged in pair in such a fashion that the leads of each lead pair have facing tips, respectively;

connecting portions each adapted to connect the facing tips of the leads included in an associated one of the lead pairs; and

an outer frame portion arranged outside the outer terminal portions and connected to the connecting lead portions in such a fashion that they form an integral structure together, thereby protecting the entire portion of the lead frame.

4. A method for fabricating a semiconductor device including a semiconductor chip, a plurality of leads fixedly attached to a terminal-end surface of the semiconductor chip by an insulating adhesive-interposed between the semiconductor chip and the leads, each of the leads including integral portions, that is, an inner terminal portion adapted to be electrically connected to an associated one of terminals of the semiconductor chip, an outer terminal portion extending outwardly in a direction orthogonal to the terminal-end surface of the semiconductor chip and adapted to be connected to an external circuit,

and a connecting lead portion adapted to connect the inner and outer terminal portions to each other; and outer electrodes each connected to the outer terminal portion of an associated one of the leads and made of solder to allow
5 the semiconductor device to be mounted on a circuit board, at least a part of the outer leads being externally exposed from a resin encapsulate, comprising the steps of:

(A) fabricating a lead frame including a plurality of leads each including integral portions, that is, an inner
10 terminal portion adapted to be electrically connected to an associated one of terminals of a semiconductor chip, an outer terminal portion adapted to be connected to an associated one of terminals of an external circuit, and a connecting lead portion adapted to connect the inner and
15 outer terminal portions to each other, each of the outer terminal portions of the leads being protruded in a direction orthogonal to a lead frame surface via an associated one of the connecting lead portions, the inner lead portions of the leads being arranged in pair in such a
20 fashion that the leads of each lead pair have facing tips, respectively, connecting portions each adapted to connect the facing tips of the leads included in an associated one of the lead pairs, and an outer frame portion arranged outside the outer terminal portions and connected to the
25 connecting lead portions in such a fashion that they form

an integral structure together, thereby protecting the entire portion of the lead frame;

(B) applying an insulating layer to a surface of the lead frame opposite to the outer terminal portions, punching out the connecting portions adapted to connect facing ones of the inner lead portions to each other along with portions of the insulating layer respectively arranged at regions corresponding to the connecting portions by use of punching dies, aligning the punched portions of the lead frame with the terminals of the semiconductor chip, and mounting the entire portion of the lead frame on the semiconductor chip by the adhesive interposed therebetween;

(C) cutting off unnecessary portions of the lead frame including the outer frame portion by use of punching dies, thereby removing the cut-off portions;

(D) wire-bonding the terminals of the semiconductor chip with tips of the inner terminal portions mounted on the semiconductor chip, and encapsulating the semiconductor chip and the lead frame by a resin while allowing a surface of the lead frame toward the outer terminal portions to be externally exposed; and

(E) forming outer electrodes made of solder on the exposed lead frame surface toward the outer terminal portions.

[DETAILED DESCRIPTION OF THE INVENTION]

[FIELD OF THE INVENTION]

The present invention relates to a resin encapsulated semiconductor device (plastic package) in which a semiconductor chip is packaged, and more particularly to a semiconductor device configured to achieve an improvement in mounting density or to have a multi-pinned structure and a method for manufacturing such a semiconductor device.

10 [DESCRIPTION OF THE PRIOR ART]

Recently, semiconductor devices have been developed to have a higher integration degree and a higher performance by virtue of developments of techniques associated with an increase in integration degree and miniaturization and in pace with the tendency of electronic appliances to have a high performance and a light, thin, simple, and miniature structure. A representative example of such semiconductor devices is an ASIC of LSI. For instance, developments of resin encapsulated semiconductor device plastic packages have been advanced from surface-mounting packages such as SOJs (Small Outlined-Leaded Packages) or QFPs (Quad Flat Packages) to packages having a miniature structure mainly achieved in accordance with a thinness obtained by virtue of developments of TSOPs (Tin Small Outline Packages) or to LOC (Lead On Chip) structures

adapted to achieve an improvement in the chip packaging efficiency by virtue of developments of an internal three-dimensional package structure. In addition to an increase in integration degree and improvement in performance, there has also been growing demand for an increase in the number of pins, thickness, and miniaturization of resin encapsulated semiconductor packages. In the above mentioned conventional packages, however, there is a limitation in miniaturization because those packages have a structure in which leads are arranged around a chip. Similarly, leads are arranged around a chip in the case of miniature packages such as TSOPs. In such packages, there is also a limitation in increasing the number of pins due to the pin pitch used.

[SUBJECT MATTERS TO BE SOLVED BY THE INVENTION]

As mentioned above, there has been demand for an increase in integration degree and improvement in performance of resin encapsulated semiconductor devices. Also, there has also been growing demand for an increase in the number of pins, thickness, and miniaturization of resin encapsulated semiconductor packages. In such situations, the present invention makes it possible to increase the occupancy degree of a chip in a semiconductor package with a limited size while reducing the mounting area of the

semiconductor package on a circuit board to achieve a miniaturization of the resulting semiconductor device. That is, the present invention is adapted to provide a resin encapsulated semiconductor device capable of achieving an improvement in the mounting density thereof on a circuit board. Also, the present invention is adapted to achieve an increase in the number of pins which is difficult in miniature packages such as conventional TSOPs.

10 (MEANS FOR SOLVING THE SUBJECT MATTERS)

The resin encapsulated semiconductor device of the present invention is characterized in that it comprises: a semiconductor chip; a plurality of leads fixedly attached to a terminal-end surface of the semiconductor chip by an insulating adhesive interposed between the semiconductor chip and the leads, each of the leads including integral portions, that is, an inner terminal portion adapted to be electrically connected to an associated one of terminals of the semiconductor chip, an outer terminal portion extending outwardly in a direction orthogonal to the terminal-end surface of the semiconductor chip and adapted to be connected to an external circuit, and a connecting lead portion adapted to connect the inner and outer terminal portions to each other; and outer electrodes each connected to the outer terminal portion of an associated one of the

leads and made of solder to allow the semiconductor device to be mounted on a circuit board, at least a part of the outer leads being externally exposed from a resin encapsulate. The above semiconductor device can be embodied into a BGA (Ball Grid Array) type resin encapsulated semiconductor device by arranging a plurality of leads each having an inner terminal portion and an outer terminal portion integral with each other in a two-dimensional fashion on the terminal-end surface of the semiconductor chip and forming the outer electrodes in the form of solder balls.

The above semiconductor device is also characterized in that the terminals of the semiconductor chip are arranged along a substantially center line between a pair of sides of the semiconductor chip on the terminal-end surface of the semiconductor chip, and the leads are arranged in two facing sets along the sides of the semiconductor chip, respectively, in such a fashion that the terminals of the semiconductor chip are interposed between the two facing lead sets. The lead frame of the present invention is characterized in that it comprises: a plurality of leads each including integral portions, that is, an inner terminal portion adapted to be electrically connected to an associated one of terminals of a semiconductor chip, an outer terminal portion adapted to be

connected to an associated one of terminals of an external circuit, and a connecting lead portion adapted to connect the inner and outer terminal portions to each other; each of the outer terminal portions of the leads being protruded in a direction orthogonal to a lead frame surface via an associated one of the connecting lead portions; the inner lead portions of the leads being arranged in pair in such a fashion that the leads of each lead pair have facing tips, respectively; connecting portions each adapted to connect the facing tips of the leads included in an associated one of the lead pairs; and an outer frame portion arranged outside the outer terminal portions and connected to the connecting lead portions in such a fashion that they form an integral structure together, thereby protecting the entire portion of the lead frame. The above lead frame can be embodied into a lead frame for a BGA (Ball Grid Array) type resin encapsulated semiconductor device by arranging a plurality of leads each having an inner terminal portion and an outer terminal portion integral with each other in a two-dimensional fashion on the terminal-end surface of the semiconductor chip and forming the outer electrodes in the form of solder balls.

The present invention is also characterized by a method for fabricating a semiconductor device including a semiconductor chip, a plurality of leads fixedly attached

to a terminal-end surface of the semiconductor chip by an insulating adhesive interposed between the semiconductor chip and the leads, each of the leads including integral portions, that is, an inner terminal portion adapted to be electrically connected to an associated one of terminals of the semiconductor chip, an outer terminal portion extending outwardly in a direction orthogonal to the terminal-end surface of the semiconductor chip and adapted to be connected to an external circuit, and a connecting lead portion adapted to connect the inner and outer terminal portions to each other; and outer electrodes each connected to the outer terminal portion of an associated one of the leads and made of solder to allow the semiconductor device to be mounted on a circuit board, at least a part of the outer leads being externally exposed from a resin encapsulate, comprising the steps of: (A) fabricating a lead frame including a plurality of leads each including integral portions, that is, an inner terminal portion adapted to be electrically connected to an associated one of terminals of a semiconductor chip, an outer terminal portion adapted to be connected to an associated one of terminals of an external circuit, and a connecting lead portion adapted to connect the inner and outer terminal portions to each other, each of the outer terminal portions of the leads being protruded in a direction orthogonal to a

lead frame surface via an associated one of the connecting lead portions, the inner lead portions of the leads being arranged in pair in such a fashion that the leads of each lead pair have facing tips, respectively, connecting portions each adapted to connect the facing tips of the leads included in an associated one of the lead pairs, and an outer frame portion arranged outside the outer terminal portions and connected to the connecting lead portions in such a fashion that they form an integral structure together, thereby protecting the entire portion of the lead frame; (B) applying an insulating layer to a surface of the lead frame opposite to the outer terminal portions, punching out the connecting portions adapted to connect facing ones of the inner lead portions to each other along with portions of the insulating layer respectively arranged at regions corresponding to the connecting portions by use of punching dies, aligning the punched portions of the lead frame with the terminals of the semiconductor chip, and mounting the entire portion of the lead frame on the semiconductor chip by the adhesive interposed therebetween; (C) cutting off unnecessary portions of the lead frame including the outer frame portion by use of punching dies, thereby removing the cut-off portions; (D) wire-bonding the terminals of the semiconductor chip with tips of the inner terminal portions mounted on the semiconductor chip, and

encapsulating the semiconductor chip and the lead frame by
a resin while allowing a surface of the lead frame toward
the outer terminal portions to be externally exposed; and
(E) forming outer electrodes made of solder on the exposed
5 lead frame surface toward the outer terminal portions.

[FUNCTIONS]

With the above mentioned configuration, the resin
encapsulated semiconductor device of the present invention
10 can increase the occupancy degree of the chip while
achieving a miniaturization thereof. That is, the resin
encapsulated semiconductor device is capable of reducing
the mounting area thereof on a circuit board and achieving
an improvement in the mounting density thereof on the
15 circuit board. In particular, the present invention
achieves a miniaturization of the semiconductor device by
fixedly attaching a plurality of leads each including an
inner terminal portion and an outer terminal portion
integral with each other to a surface of a semiconductor
20 chip by an insulating adhesive layer interposed between the
semiconductor chip and the leads, and connecting outer
electrodes made of solder to the outer terminal portions,
respectively. Also, the present invention achieves an
increase in the number of pins in the semiconductor device
25 by arranging the outer electrodes made of solder in a two-

dimensional fashion on a plane parallel to the surface of the semiconductor chip. Where the outer electrodes made of solder are formed in the form of solder balls and arranged in a two-dimensional fashion, a BGA type semiconductor device capable of achieving an increase in the number of pins can be obtained. In the above semiconductor device, the terminals of the semiconductor chip are arranged along a substantially center line between a pair of sides of the semiconductor chip on the terminal-end surface of the semiconductor chip, and the leads are arranged in two facing sets along the sides of the semiconductor chip, respectively, in such a fashion that the terminals of the semiconductor chip are interposed between the two facing lead sets. Thus, the semiconductor device has a simple structure suitable in regard to productivity. The lead frame of the present invention makes it possible to fabricate the above mentioned resin encapsulated semiconductor device by virtue of there above mentioned configuration thereof. However, this lead frame can be fabricated using a half etching method during an etching process as used for conventional lead frames. The method for fabricating a resin encapsulated semiconductor device in accordance with the present invention involves the steps of applying an insulating layer to a surface of the lead frame opposite to the outer terminal portions, punching out

the connecting portions adapted to connect facing ones of the inner lead portions to each other along with portions of the insulating layer respectively arranged at regions corresponding to the connecting portions by use of punching dies, aligning the punched portions of the lead frame with the terminals of the semiconductor chip, and mounting the entire portion of the lead frame on the semiconductor chip by the adhesive interposed therebetween, and cutting off unnecessary portions of the lead frame including the outer frame portion by use of punching dies, thereby removing the cut-off portions. Thus, a plurality of leads each including an inner terminal portion and an outer terminal portion integral with each other are mounted on a semiconductor chip. Accordingly, the present invention makes it possible to achieve a miniaturization of semiconductor devices. In accordance with the present invention, it is also possible to fabricate a resin encapsulated semiconductor device having an increased number of pins.

(EMBODIMENTS)

Hereinafter, embodiments of the present invention associated with resin encapsulated semiconductor devices will be described in conjunction with the annexed drawings.

Fig. 1A is a cross-sectional view schematically

illustrating a resin encapsulated semiconductor device according to an embodiment of the present invention. Fig. 1B is a perspective view illustrating an essential part of the resin encapsulated semiconductor device. Figs. 1A and 5 1B, the reference numeral 100 denotes the resin encapsulated semiconductor device, 101 a semiconductor chip, 102 leads, 102A inner terminal portions, 102B outer terminal portions, 102C connecting lead portions, 101A contacts (pads), 103 wires, 104 an insulating adhesive, 105 a resin encapsulate, 106 outer electrodes made of solder (paste), respectively. The resin encapsulated semiconductor device according to this embodiment is fabricated using a lead frame which will be described hereinafter. In this resin encapsulated semiconductor device, a plurality of L-shaped leads 102, each of which 15 has an inner terminal portion 102A and an outer terminal portion 102 integral with each other, are mounted on a semiconductor chip 101 by means of an insulating adhesive 104. An outer electrode 106, which is made of solder, is 20 attached to each outer terminal portion 102B. The outer electrode 106 is outwardly protruded from a resin encapsulate 105. The resin encapsulated semiconductor device configured as mentioned above has a package area substantially equal to the entire area thereof. When this 25 semiconductor device is mounted on a circuit board, the

solder is melted and then solidified to allow the outer terminal portions 102B to be electrically connected to an external circuit. In the resin encapsulated semiconductor device according to the illustrated embodiment, contacts (pads) 101A provided at the semiconductor chip 101 are arranged in pairs along a center line L of the semiconductor chip 101 at opposite sides of the center line L in such a fashion that contacts included in each contact pair face each other. The outer terminal portion 102B of each lead is spaced apart from the inner terminal portion 102A of the lead. Between the inner and outer terminal portions 102A and 102B, a connecting lead portion 102C is interposed. The connecting lead portion 102C of each lead is bent in a direction orthogonal to the major surface of the semiconductor chip at a position near an associated one of the side surfaces of the semiconductor chip 101, so that it has an L shape. In each lead, the outer terminal portion 102B is arranged at an end of the connecting lead portion 102C. The outer terminal portions 102B of the leads are arranged in a one-dimensional fashion on a plane parallel to the major surface of the semiconductor chip 101. That is, the outer terminal portions 102B are arranged in two lines at opposite sides of the center line L. As mentioned above, one outer electrode 106 made of solder is connected to the outer terminal portion 102B of

each lead and outwardly exposed from the resin encapsulate
105.

For the insulating adhesive 104, a polyimide-based thermoplastic adhesive having a thickness of 100 μm (HM122C
5 manufactured by Hitachi Chemical Co., Ltd.) is preferably used. Alternatively, a silicon denaturalized polyimide adhesive (ITA1715 manufactured by Sumitomo Bakelite Co., Ltd.) or a thermosetting adhesive (HG5200 manufactured by Tomoekawa Papermaking Co., Ltd.) may be used. Although
10 outer electrodes made of solder paste are used in the illustrated embodiment, solder balls may be used.

As mentioned above, the resin encapsulated semiconductor device according to the illustrated embodiment has a package area substantially equal to the
15 entire area thereof. That is, the illustrated embodiment of the present invention provides a package having a compact structure in regard to area. In accordance with the present invention, a thinned package structure can also be provided in that it is also possible to reduce the
20 package thickness to about 1.0 mm or less. Although the outer electrodes have been described as being arranged in two lines along the contacts (pads) of the semiconductor chip, they may be arranged in a two-dimensional fashion. This is achieved by arranging contacts of the semiconductor
25 chip in a two-dimensional fashion. On the surface of the

semiconductor chip arranged with those contacts, a plurality of terminal sets each having an inner terminal and outer terminal integral with each other are arranged in a two-dimensional fashion. In this case, it is possible to
5 fabricate a semiconductor device using a semiconductor chip with an increased number of pins.

An embodiment of the present invention associated with a lead frame will now be described. The lead frame according to this embodiment is adapted to be used in the
10 above mentioned semiconductor device. Fig. 2 is a plan view of the lead frame according to this embodiment. In Fig. 2, the reference numeral 200 denotes a lead frame, 201 inner terminal portions, 202 outer terminal portions, 203 connecting lead portions, 204 a connecting portion, and 205
15 an outer frame portion, respectively. The lead frame is made of 42 ALLOY (namely, an Fe alloy containing 42% Ni). The lead frame has a thickness of 0.05 mm at its thinner portion, that is, the inner terminal portions, and a thickness of 0.2 mm at its thicker portion, that is, the
20 outer terminal portions. The connecting portion, which connects facing tips of the inner terminal portions to each other, has a thickness of 0.05 mm corresponding to that of the thinner portion. This connecting portion has a
25 structure capable of allowing an easy punching thereof in the fabrication of the semiconductor device, as described

hereinafter. Although the outer terminal portions 202 have a ball shape in the illustrated embodiment, they are not limited to this shape. Also, although the lead frame has been described as being made of the 42 ALLOY, it is not limited to this material. For the lead frame, a copper-based alloy may be used.

Now, fabrication of the lead frame according to the illustrated embodiment will be described in brief. Fig. 4 illustrates a process for fabricating the lead frame according to the illustrated embodiment. First, a lead frame blank 300 having a thickness of 0.2 mm was prepared which is made of a 42 ALLOY (an Fe alloy containing 42% Ni). The prepared lead frame blank 300 was then subjected to a cleaning process, thereby removing grease from the surfaces thereof (Fig. 3a). Subsequently, photoresist films 301 were coated over both surfaces of the lead frame blank 300, respectively. The coated photoresist films 301 were then dried (Fig. 3b).

Using desired pattern plates, the photoresist films 301 on both surfaces of the lead frame blank 300 were exposed to light at their desired portions. A developing process was then conducted to the light-exposed photoresist films 301, thereby forming photoresist patterns 301A.

For the photoresist films, a negative liquid-phase resist (PMER resist) manufactured by Tokyo Ohka Co., Ltd.

was used. Using the resist patterns 301A as anti-etch films, the lead frame blank 300 was subjected to a spray etching process at both surfaces thereof. The spray etching process was conducted using a ferric chloride solution of 48 BAUME at 57 °C. Thus, a lead frame having a structure of Fig. 2a was obtained (Fig. 3d). Fig. 2a is a plan view of the lead frame. Fig. 2b is a cross-sectional view taken along the line A1 - A2 of Fig. 2a. Thereafter, the remaining photoresist thin films were peeled off. The resulting structure was then subjected to a cleaning process. A gold plating process was subsequently conducted for desired portions of the lead frame, that is, regions including inner terminal portions (Fig. 3e).

In the fabrication process of the lead frame, the etching process was conducted with a large etch depth at one major surface of the lead frame blank where outer terminal portions are to be formed, and with a small etch depth at the other major surface of the lead frame. In place of the gold plating, silver or palladium plating may be utilized. The above mentioned lead frame fabrication process is adapted to manufacture a single lead frame required for the manufacture of a single semiconductor device. In terms of productivity, however, the etching process is conducted for lead frame units each corresponding to the single lead frame shown in Fig. 2. To

this end, a frame member (not shown) is provided at a desired portion of the peripheral edge of the lead frame so as to connect a desired part of the outer frame portion 205 shown in Fig. 2 to a corresponding one of an adjacent lead frame.

Using the lead frame fabricated as mentioned above, the resin encapsulated semiconductor device according to the present invention was fabricated. Now, a method for fabricating the resin encapsulated semiconductor device in accordance with an embodiment of the present invention will be described. Fig. 4 illustrates the method for fabricating the resin encapsulated semiconductor device in accordance with the embodiment of the present invention. A polyimide-based thermosetting insulating adhesive (tape) 401 (HM122C manufactured by Hitachi Chemical Co., Ltd.) was applied to one surface, formed with the outer terminal portions 402, of the lead frame 400 fabricated as in Fig. 3 and the outer surface of the lead frame 400 using a hot pressing process conducted at 400 °C and 6 Kg/m² for 1.0 second Fig. 4a). The resulting structure is shown in Fig. 5 which is a plan view. Thereafter, the connecting portions 403 connecting facing tips of the inner terminal portions were punched using punching dies 405A and 405B (Fig. 4b). Also, portions of the insulating adhesive

(tape) corresponding to those connecting portions 403 were punched (Fig. 4c).

Subsequently, unnecessary portions of the lead frame including the outer frame 404 were cut off using outer frame punching and pressing dies 406A and 406B (Fig. 4d).
5 The lead frame was then bonded to a semiconductor chip 407 at its leads 410 under pressure while applying heat (Fig. 4e).

The process for cutting off the unnecessary portion of the lead frame including the outer frame 404 supporting
10 the entire portion of the lead frame along with the connecting lead portion, as shown in Fig. 4d, may be carried out after an resin encapsulating process. In this case, dam bars (not shown) are preferably provided, as in
15 QFP packages typically using a lead frame having a single layer structure. After the mounting of the leads 410 on the semiconductor chip 411, the inner terminal portion 410 of each lead 410 was electrically connected to an associated one of terminals (pads) 411A of the
20 semiconductor chip 411 (Fig. 4f).

Subsequently, an epoxy-based resin 415 was molded to encapsulate the resulting structure while exposing the outer terminal portions 410B of the leads 410 using a desired mold (Fig. 4g).

Although a specific mold (not shown) was used for the above process in the illustrated case, use of such a die may be unnecessary in so far as the resin encapsulating process can be conducted under the condition in which
5 desired portions (outer terminal portions) of the lead frame are left. Thereafter, a solder paste was coated on the exposed outer terminal portions 410B in accordance with a screen printing process, thereby forming outer electrodes
416 made of solder (paste). Thus, the fabrication of the
10 resin encapsulated semiconductor device according to the present invention was achieved (Fig. 4h).

Although the formation of the outer electrodes 416 made of solder has been described as being achieved using a screen printing process, it may be achieved using a reflow
15 or bonding process in so far as an amount of solder required for a connection of the semiconductor device to a circuit board is obtained.

(EFFECTS OF THE INVENTION)

20 As apparent from the above description, the present invention makes it possible to increase the occupancy degree of a semiconductor chip in a semiconductor package in situations requiring new resin encapsulated
semiconductor devices having a highly integrated structure
25 while exhibiting a high performance. The present invention

also makes it possible to reduce the area of the semiconductor device on a circuit board in order to cope with a compactness of the semiconductor device. That is, the present invention can provide a semiconductor device
5 capable of achieving an improvement in the mounting density on a circuit board. At the same time, the present invention can provide a resin encapsulated semiconductor device having a new multipinned structure which could not be realized in compact packages such as conventional TSOPs.